Midterm Exam

(October 19th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (20 PTS)

a) Complete the following table. The decimal numbers are unsigned: (5 pts.)

Decimal	BCD	Binary	Reflective Gray Code
37			
			101011
	000100101000		

b) Complete the following table. The decimal numbers are signed. Use the fewest number of bits in each case: (12 pts.)

	REPRESENTATION		
Decimal	**Sign-and-magnitude**	**1's complement**	**2's complement**
	110001		
			1000000
-32			
			101000
			0101001
		1011011	

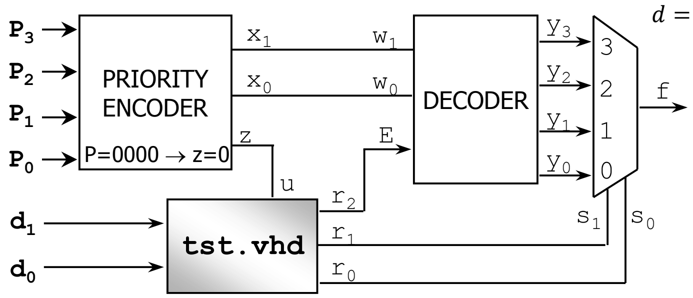
c) Convert the following decimal numbers to their 2's complement representations. (3 pts)

- ✓ -17.125
- ✓ 32.375

PROBLEM 2 (15 PTS)

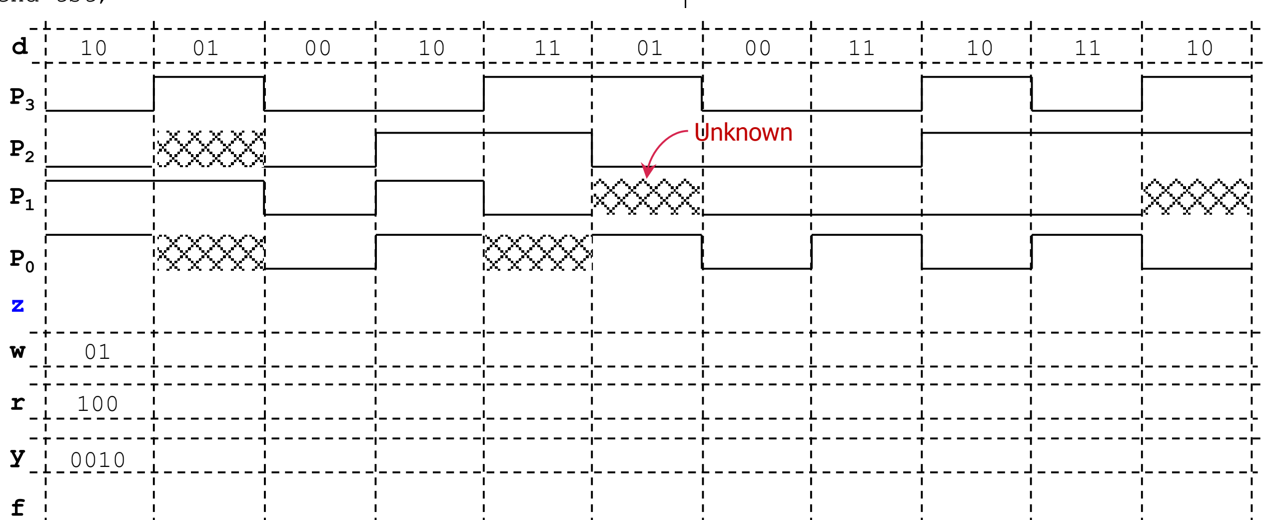
- Complete the timing diagram of the following circuit. The VHDL code (`tst.vhd`) corresponds to the shaded circuit.

$d = d_1d_0,\ w = w_1w_0,\ r = r_2r_1r_0,\ y = y_3y_2y_1y_0$



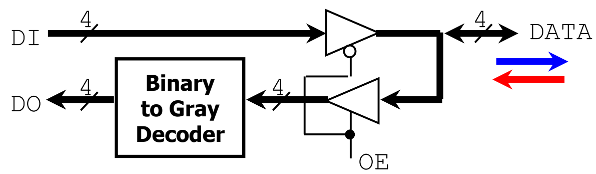

```
library ieee;
use ieee.std_logic_1164.all;
entity tst is
  port (d: in std_logic_vector(1 downto 0);
        r: out std_logic_vector(2 downto 0);
        u: in std_logic);
end tst;
```

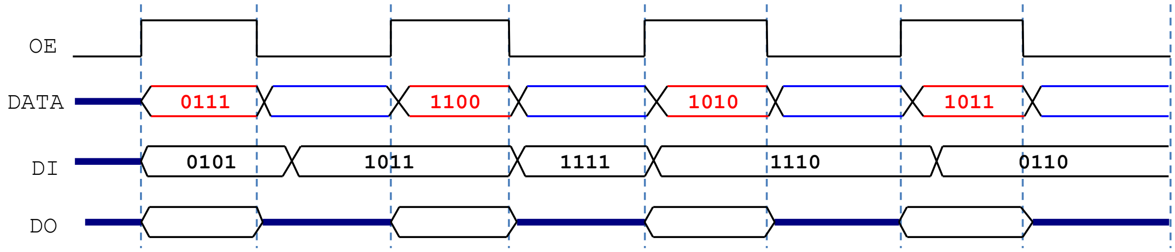
```
architecture bhv of tst is

begin

  process (d, u)
  begin

     r <= '1'&d;
     if u = '1' then
        r <= d&'0';
     end if;

  end process;

end bhv;
```



PROBLEM 3 (8 PTS)

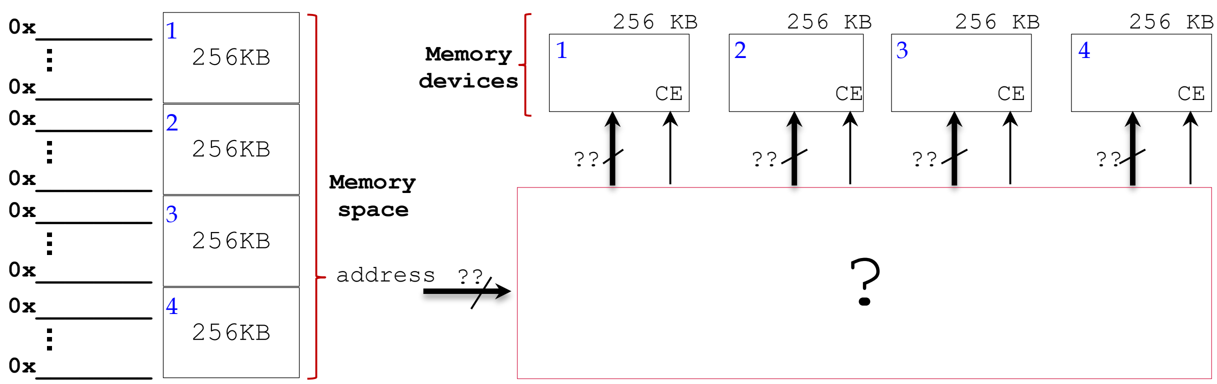
- Complete the timing diagram (signals DO and $DATA$) of the following circuit. The 4-bit binary to gray decoder treats input data as unsigned numbers.





PROBLEM 4 (12 PTS)

- A microprocessor has a memory space of 1 MB. Each memory address occupies one byte. 1KB = 2^{10} bytes, 1MB = 2^{20} bytes, 1GB = 2^{30} bytes. We want to connect four 256 KB memory chips to this microprocessor.
  - ✓ What is the address bus size (number of bits of the address) of the microprocessor? (1 pt).
  - ✓ For a memory chip of 256 KB, how many bits do we require to address 256 KB of memory? (1 pt).
  - ✓ Complete the address ranges (lowest to highest, in hexadecimal) for each of the memory chips in the figure. (4 pts).
  - ✓ Sketch the circuit that: i) addresses the memory chips, and ii) enables only one memory chip (via CE: chip enable) when the address falls in the corresponding range. Example: if `address=0x5FFFF`, → only memory chip 2 is enabled (CE=1). If `address=0xD0123`, → only memory chip 4 is enabled.



PROBLEM 5 (17 PTS)

a) Perform the following additions and subtractions of the following unsigned integers. Use the fewest number of bits n to represent both operators. Indicate every carry (or borrow) from c_0 to c_n (or b_0 to b_n). For the addition, determine whether there is an overflow. For the subtraction, determine whether we need to keep borrowing from a higher byte. (6 pts)
   - ✓ `17 + 50`
   - ✓ `37 - 41`

b) Perform the following operations, where numbers are represented in 2's complement. Indicate every carry from c_0 to c_n. For each case, use the fewest number of bits to represent the summands and the result so that overflow is avoided. (8 pts)
   - ✓ `-36 + 50`
   - ✓ `-41 - 24`

c) Perform binary multiplication of the following numbers that are represented in 2's complement arithmetic. (3 pts)
   - ✓ `-7 x 9`

PROBLEM 6 (10 PTS)

- Given two 4-bit <u>unsigned</u> numbers A, B, sketch the circuit that computes $|A - 2B|$. For example: $A = 1010, B = 1110 \rightarrow |A - 2B| = |10 - 2 \times 14| = 18$. You can only use full adders and logic gates. Your circuit must avoid overflow: design your circuit so that the result and intermediate operations have the proper number of bits.

PROBLEM 7 (18 PTS)

- Sketch the circuit that implements the following Boolean function: $f(a, b, c, d) = (a \oplus \bar{b})(c \oplus d)$
  - ✓ Using <u>ONLY</u> 2-to-1 MUXs (AND, OR, NOT, XOR gates are not allowed). (12 pts)
  - ✓ Using two 3-to-1 LUTs and a 2-to-1 MUX. Specify the contents of each of the 3-to-1 LUTs. (6 pts)